CLAIMS:

1. A method, comprising:

a) issuing a load with reservation instruction including a requested address to a shared memory at which data may be located;

b) receiving the data from the shared memory such that any operations may be performed on the data;

c) at least one of: (i) entering a low power consumption mode, and (ii) initiating another processing task; and

d) receiving notification that the reservation was lost, the reservation being lost when the data at the address in shared memory is modified.

2. The method of claim 1, wherein the notification that the reservation was lost operates as an interrupt that at least one of (i) interrupts the low power consumption mode; and (ii) interrupts the other processing task.

3. The method of claim 1, wherein the step of entering the low power consumption mode or the step of initiating another processing task is carried out only if the data is not a predetermined value.

4. The method of claim 3, further comprising repeating steps a) through d) when the notification indicates that the reservation was lost.

5. The method of claim 1, further comprising: writing an identification number, associated with a processor issuing the load with reservation instruction, into a status location associated with the addressed location in the shared memory when the data is accessed from the shared memory.

6. The method of claim 1, further comprising: causing a reservation lost bit in a status register of the processor to indicate that the reservation was lost when the data at the address in shared memory is modified.

7. The method of claim 6, wherein the step of determining whether the reservation was lost includes polling the status register and determining that the reservation was lost when the reservation lost bit so indicates.

8. A system, comprising:

a shared memory;

a memory interface unit operatively coupled to the shared memory; and

a plurality of processing units in communication with the memory interface, at least one of the processing units being operable to:

a) issue a load with reservation instruction to the memory interface unit, the load with reservation instruction including a requested address to the shared memory at which data may be located;

b) receive the data from the memory interface unit such that any operations may be performed on the data;

c) at least one of: (i) enter a low power consumption mode, and (ii) initiate another processing task; and

d) receive notification that the reservation was lost, the reservation being lost when the data at the address in shared memory is modified.

9. The system of claim 8, wherein the notification that the reservation was lost operates as an interrupt that at least one of (i) interrupts the low power consumption mode; and (ii) interrupts the other processing task.

10. The system of claim 8, wherein the at least one processing unit is operable to enter the low power consumption mode or initiate the other processing task only if the data is not a predetermined value.

11. The system of claim 10, wherein the at least one processor is further operable to repeat steps a) through d) when the notification indicates that the reservation was lost.

12. A system, comprising:

a shared memory;

a memory interface unit coupled to the shared memory and operable to retrieve data from the shared memory at requested addresses, and to write data to the shared memory at requested addresses; and

a plurality of processing units in communication with the memory interface and operable to instruct the memory interface unit that data be loaded with reservation from the shared memory at a specified address such that any operations may be performed on the data,

wherein at least one of the processing units includes a status register having one or more bits indicating whether a reservation was lost, the reservation being lost when the data at the specified address in shared memory is modified by another one or more of the processing units.

13. The system of claim 12, wherein the at least one processing unit is operable to enter a low power consumption mode if the data is not a predetermined value.

14. The system of claim 13, wherein the at least one processing unit is further operable to exit the low power

consumption mode in response to an event that is permitted to interrupt the low power consumption mode.

15. The system of claim 14, wherein the at least one processing unit is further operable to poll the one or more bits of the status register to determine whether the reservation was lost.

16. The system of claim 15, wherein the at least one processing unit is further operable to (i) re-instruct the memory interface unit to load the data with reservation from the shared memory at the specified address such that any operations may be performed on the data.

17. The system of claim 14, wherein the event that is permitted to interrupt the low power consumption mode is that the reservation was lost.

18. The system of claim 11, wherein the memory interface unit is operable to write an identification number, associated with the at least one processing unit issuing the load with reservation instruction, into a status location associated with the specified address of the shared memory when the data is accessed from the shared memory.

19. The system of claim 12, wherein the memory interface unit is operable to monitor whether the reservation is lost by monitoring whether the data at the specified address in shared memory is modified by another of the processing units.

20. The system of claim 19, wherein the memory interface unit is operable to cause the one or more bits of the status register of the at least one processing unit to indicate that the reservation was lost.

21. A system, comprising:

a shared memory;

a memory interface unit coupled to the shared memory and operable to retrieve data from the shared memory at requested addresses, and to write data to the shared memory at requested addresses; and

a plurality of processing units in communication with the memory interface and operable to (i) instruct the memory interface unit that data be loaded with reservation from the shared memory at a specified address such that any operations may be performed on the data,

wherein at least one processing unit is operable to at least one of: (i) enter into a low power consumption mode after issuing the instruction that the data be stored in the shared memory at the specified address; and (ii) initiate another processing task.

22. The system of claim 21, wherein the at least one processing unit is operable to enter the low power consumption mode or initiate the other processing task only if the data is not a predetermined value.

23. The system of claim 21, wherein the at least one processing unit is further operable to at least one of (i) exit the low power consumption mode, and (ii) suspend the other processing task, in response to an indication that the reservation was lost.

24. The system of claim 21, wherein the at least one processing unit includes a status register having one or more bits indicating whether a reservation was lost, the reservation being lost when the data at the specified address in shared memory is modified.

25. The system of claim 24, wherein the memory interface unit is operable to cause the one or more bits of the status register of the at least one processing unit to indicate that the reservation was lost.

26. The system of claim 24, wherein the at least one processing unit is further operable to poll the one or more bits of the status register to determine whether the reservation was lost.

27. The system of claim 25, wherein the at least one processing unit is further operable to (i) re-instruct the memory interface unit to load the data with reservation from the shared memory at the specified address such that any operations may be performed on the data.

28. The system of claim 21, wherein the memory interface unit is operable to write an identification number, associated with the at least one processing unit issuing the load with reservation instruction, into a status location associated with the specified address of the shared memory when the data is accessed from the shared memory.

29. A system, comprising:

a shared memory;

a memory interface unit operatively coupled to the shared memory; and

a plurality of N processing units in communication with the memory interface, the processing units being operable to execute a plurality of tasks in parallel using barrier synchronization by:

a) performing one of the plurality of tasks;

b) initializing a local variable, w;

c) issuing a load with reservation instruction to the memory interface unit to load a shared variable, s, from the shared memory into the local variable w;

d) incrementing or decrementing the local variable w toward the value of N;

e) issuing a store conditionally instruction to the memory interface unit to facilitate storage of the value of the local variable w as the shared variable s in the shared memory;

f) repeating steps a)-e) if the reservation is lost, the reservation being lost when the shared variable at the address in shared memory is modified;

g) issuing a store instruction to the memory interface unit to facilitate storage of a target value as the shared variable s in the shared memory when the value of the local variable reaches N;

h) issuing a load with reservation instruction to the memory interface unit to load the shared variable s from the shared memory into the local variable w;

i) entering a low power consumption mode, or initiating another processing task, when the value of the local variable is not the target value otherwise skip to step k);

j) exiting the low power consumption mode, or suspending the other processing task, and repeat steps h)-i) upon receipt of notification that the reservation was lost, the reservation being lost when a request for the shared variable in the shared memory is made by another processor; and

k) performing a next one of the plurality of tasks.